

REMARKS

I. Introduction

Claims 11 to 20 are pending in the present application. Applicants hereby respectfully request further examination and reconsideration of the application based on the following explanation.

Applicants thank the Examiner for acknowledging the claim for foreign priority and indicating that all certified copies of the priority documents have been received.

II. Objection to the Drawings under 37 CFR 1.83(a)

The drawings were objected to under 37 CFR 1.83(a). Figures 1 and 2 have been amended by adding the label “Logic Circuit Unit” for block 11 and adding the label “AND Gate” for block 10. No new matter has been added, and the Replacement Sheets are supported by the present application, including the specification. Entry and approval is respectfully requested.

With respect to the inclusion of the label “Logic Circuit Unit” for block 11, the specification indicates at page 5, lines 5-6, that “[t]he output signal of block 10 is supplied to block 11 which represents a logic circuit unit and which may be implemented using flip-flops,” and the specification further indicates at page 4, lines 38-40, that “[a]ccording to the present invention, the redundant hardware path is implemented by using logic modules. Such logic modules include gates and flip-flops, i.e., multivibrator circuits.” Accordingly, block 11 clearly represents a logic module including at least one of a gate and a flip-flop.

With respect to the inclusion of the label “AND Gate” for block 10, the specification indicates, at page 4, line 28 - page 5, line 4, the following:

Block 10 enables the activation of the airbag triggering circuits as a function of the status of the deactivation switch and combines this with an additional enable signal from processor 9 to enable airbag output stages 12 by processor 9 before, in the event of a crash, deployment should indeed take place, regardless of whether the deactivation switch is in the ‘on’ or ‘off’ position. However, due to block 10, microcontroller 9 may activate output stages 12 via safety semiconductor 13 only

when deactivation switch 1 is also in the 'on' position. If deactivation switch 1 is in the 'off' position, then output stages 12 are deactivated independently of the processor enabling line to block 10. Particularly in airbag control units having a DC ignition, this function may represent an additional protection against erroneous deployment in the event of defects in output stage IC 12.

In addition, the specification further indicates at page 5, lines 28-30, that "[a]s described above, processor 9 itself is connected to block 10 via an enable line to establish an AND gate, as well as to block 11 to influence the time response." As described in the specification, block 10 enables the activation of triggering circuits. Due to block 10, the processor 9 may activate the triggering circuits only when the deactivation switch is also in the "on" position. Block 10 reads the status of the deactivation switch from module 8. In addition, the first block diagram of Fig. 1 clearly shows block 10 receiving signals from processor 9 and module 8, and sending signals through logic circuit unit 11 to safety semiconductor 13, which is connected to output stages 12, which are in turn connected to triggering circuits 15 through 18. Accordingly, block 10 clearly represents an AND gate connectible to triggering circuit control, wherein the module and the processor are connected to the AND gate.

For at least the foregoing reasons, withdrawal of the drawing objection is requested.

III. Rejection of Claims 11-20 under 35 U.S.C. §112, ¶1

Claims 11-20 were rejected under 35 U.S.C. §112, ¶1, as failing to comply with the enablement requirement. Applicants respectfully submit that the rejection should be withdrawn for at least the following reasons.

Contrary to the examiner's contention that there is no disclosure showing how a switch position is verifiable by the module, the specification does clearly describe the feature of a switch position verifiable by the module in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. An applicable portion of the specification (page 4, lines 7-22) is reproduced below:

Figure 1 shows the protective device according to an exemplary embodiment of the present invention in a first block diagram. The protective device according to the exemplary embodiment of the present invention has an airbag

deactivation switch 1 and an airbag control unit 4 which are connected to one another. Airbag deactivation switch 1 has two Hall sensors 2 and 3 which are interconnected on an electrode where they receive power from control unit 4 and a current limiter 6. Current limiter 6 itself is supplied by battery voltage 5. On the other side, Hall sensor 2 is connected to two components of control unit 4. One is a module 7 which includes the voltage supply, communication interfaces, analog inputs, and an analog-to-digital converter. **The other is a module 8 which processes and analyzes the signal of Hall sensor 2. Processing of the sensor signals forks into two paths here. The digitized Hall signal is transmitted to microcontroller 9 via module 7, the microcontroller processing the signal to determine whether the deactivation switch has been operated or not. At the same time, module 8 performs the same procedure, module 8 also having access to an analog-to-digital converter in order to execute a digital analysis. The other electrode of Hall sensor 2 is also connected to module 7 and module 8 to provide redundant processing of the Hall sensor signals.**

In contrast to the Examiner's contention that there is no disclosure showing how a switch position is verifiable by the module, the specification clearly explains how the switch position is verifiable by the module. First, it is noted that processing of the sensor signal forks into two paths. The digitized Hall signal is transmitted to microcontroller 9, which processes the signal to determine whether the deactivation switch has been operated or not, i.e., in this manner a switch position is verifiable by the microcontroller. The specification further indicates that "[a]t the same time, **module 8 performs the same procedure**, **module 8 also having access to an analog-to-digital converter in order to execute a digital analysis**," (page 4, lines 18-20), i.e., module 8 performs the same procedure as the microcontroller. Therefore, the specification clearly indicates that **the switch position is verifiable by the module in the same way as the switch position is verifiable by the microcontroller**. The specification further adds that the module also has access to an analog-to-digital converter in order to execute a digital analysis.

For at least the foregoing reasons, how a switch position is verifiable by the module is clearly explained in the specification, and it is respectfully submitted that the 35 U.S.C. §112, ¶1, rejection of claim 11 and its dependent claims 12-20 should be withdrawn. Reversal of this rejection is therefore respectfully requested.

IV. Rejection of Claims 11-13 and 17-20 under 35 U.S.C. §102(b)

Claims 11-13 and 17-20 were rejected under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 5,513,878 (“Ueda”). Applicants respectfully submit that the rejection should be withdrawn for at least the following reasons.

To anticipate a claim under § 102(b), a single prior art reference must identically disclose each and every claim element. See Lindeman Maschinenfabrik v. American Hoist and Derrick, 730 F.2d 1452, 1458 (Fed. Cir. 1984). If any claimed element is absent from a prior art reference, it cannot anticipate the claim. See Rowe v. Dror, 112 F.3d 473, 478 (Fed. Cir. 1997). Anticipation requires the presence in a single prior art reference disclosure of each and every element of the claim invention, arranged exactly as in the claim. Lindeman, 703 F.2d 1458 (Emphasis added). Additionally, not only must each of the claim limitations be identically disclosed, an anticipatory reference must also enable a person having ordinary skill in the art to practice the claimed invention, namely the inventions of the rejected claims, as discussed above. See Akzo, N.V. v. U.S.I.T.C., 1 U.S.P.Q.2d 1241, 1245 (Fed. Cir. 1986). To the extent that the Examiner may be relying on the doctrine of inherent disclosure for the anticipation rejection, the Examiner must provide a “basis in fact and/or technical reasoning to reasonably support the determination that the allegedly inherent characteristics necessarily flow from the teachings of the applied art.” (See M.P.E.P. § 2112; emphasis in original; see also Ex parte Levy, 17 U.S.P.Q.2d 1461, 1464 (Bd. Pat. App. & Inter. 1990)).

Claim 11 includes the feature of **an additional module having at least one logic module, wherein a switch position is verifiable by the processor and by the additional module independently from one another**. Examiner explicitly admits that “Ueda et al. does not disclose an additional module having at least one logic module, wherein a switch position is verifiable by the additional module.” Since the Examiner explicitly admits that the above-recited feature of claim 11 is absent from the prior art Ueda reference, claim 11 cannot be anticipated by the Ueda reference.

For at least these reasons, it is respectfully submitted that claim 11 and its dependent claims 12, 13 and 17-20 are allowable over Ueda. Reversal of this anticipation rejection is therefore respectfully requested.

V. Rejection of Claim 14 under 35 U.S.C. §103(a)

Claim 14 was rejected under 35 U.S.C. §103(a) as being unpatentable over the “Ueda” reference in view of U.S. Patent Publication No. 2004-0045760 A1 (“Baumgartner”). Applicants respectfully submit that the rejection should be withdrawn for at least the following reasons.

In rejecting a claim under 35 U.S.C. § 103(a), the Examiner bears the initial burden of presenting a *prima facie* case of obviousness. In re Rijckaert, 9 F.3d 1531, 1532, 28 U.S.P.Q.2d 1955, 1956 (Fed. Cir. 1993). In addition, as clearly indicated by the Supreme Court, it is “important to identify a reason that would have prompted a person of ordinary skill in the relevant field to combine the [prior art] elements” in the manner claimed. See KSR Int’l Co. v. Teleflex, Inc., 127 S. Ct. 1727 (2007). To the extent that the Examiner may be relying on the doctrine of inherent disclosure in support of the obviousness rejection, the Examiner must provide a “basis in fact and/or technical reasoning to reasonably support the determination that the allegedly inherent characteristic necessarily flows from the teachings of the applied art.” (See M.P.E.P. § 2112; emphasis in original; see also Ex parte Levy, 17 U.S.P.Q.2d 1461, 1464 (Bd. Pat. App. & Inter. 1990)).

Applicants note that claim 14 ultimately depends on claim 11. Even if it were proper to combine the applied references as suggested by the Examiner (which is not conceded), the secondary Baumgartner reference does not cure the critical deficiencies of the Ueda reference (as explained above) with respect to base claim 11. Indeed, the Office Action merely uses Baumgartner for the alleged disclosure of a time response modification. Accordingly, claim 11 and its dependent claim 14 are patentable over the teachings of Ueda and Baumgartner. Therefore, reversal of the obviousness rejection of claim 14 is requested.

VI. Rejection of Claims 15 and 16 under 35 U.S.C. §103(a)

Claims 15 and 16 were rejected under 35 U.S.C. §103(a) as being unpatentable over the “Ueda” reference in view of U.S. Patent No. 5,570,903 (“Meister”). Applicants respectfully submit that the rejection should be withdrawn for at least the following reasons.

Applicants note that claims 15 and 16 ultimately depend on claim 11. Even if it were proper to combine the references as suggested by the Examiner (which is not conceded), the

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secondary Meister reference does not cure the critical deficiencies of the Ueda reference (as explained above) with respect to base claim 11. Indeed, the Office Action merely uses Meister for the alleged disclosure of a resistor network and a Hall-effect sensor. Accordingly, claim 11 and its dependent claims 15 and 16 are patentable over the teachings of Ueda and Meister. Therefore, reversal of the obviousness rejection of claims 15 and 16 is requested.

Conclusion

In view of the foregoing, it is respectfully submitted that pending claims 11 to 20 are in condition for allowance. All issues raised by the Examiner having been addressed, an early and favorable action on the merits is respectfully requested.

Respectfully submitted,

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